What is claimed is

1. A cyclic redundancy check (CRC) verification apparatus having constant delay, comprising:

a data buffer which stores an input data frame;

a control information buffer which stores control information on the data frame;

a CRC generation unit which performs CRC verification of the data frame;

an input control unit which receives an input control signal, generates a CRC enable signal, sends the CRC enable signal to the CRC generation unit, generates information on a write address which increases sequentially irrespective of the input of the data frame, sends the write address information to the data buffer and the control information buffer, and with storing an address in which the start part of the data frame is stored, if input of the data frame finishes, receives the CRC verification result from the CRC generation unit and stores the CRC verification result in the address in which the start part of the data frame is stored, and provides a read address synchronization signal that makes a read address follows with a predetermined offset after the write address; and

an output control unit which receives the read address synchronization signal, generates the read address which increases sequentially, sends the read address to the data buffer and the control information buffer, reads data stored in the data buffer, and outputs a different output control signal together with the data according to the CRC result.

2. The apparatus of claim 1, wherein the control information includes information on the start of the data frame, end information, buffer enable information and CRC verification result information.

3. The apparatus of claim 1, further comprising:

a retiming unit which retimes data according to a command from the output control unit, by outputting data '0' when there is no input data frame, or by not latching data in the data buffer.

4. A CRC verification apparatus having constant delay, comprising:

a buffer which stores an input data frame and control information on a data frame;

a CRC generation unit which performs CRC verification of the data frame;

an input control unit which receives an input control signal, generates a CRC enable signal, sends the CRC enable signal to the CRC generation unit, generates information on a write address which increases sequentially irrespective of the input of the data frame, sends the write address information to the buffer, and with storing an address in which the start part of the data frame is stored, if input of the data frame finishes, receives the CRC verification result from the CRC generation unit and stores the CRC verification result in the address in which the start part of the data frame is stored, and provides a read address synchronization signal that makes a read address follows with a predetermined offset after the write address; and

an output control unit which receives the read address synchronization signal, generates the read address which increases sequentially, sends the read address information to the buffer, reads data stored in the buffer, and outputs a different output control signal together with the data according to the CRC result.

5. The apparatus of claim 1, wherein the predetermined offset is the same value as the maximum length of the data frame or a value exceeding the maximum length by a predetermined degree.

6. The apparatus of claim 4, wherein the predetermined offset is the same value as the maximum length of the data frame or a value exceeding the maximum length by a predetermined degree.

7. A CRC verification apparatus having constant delay, comprising:

an input control unit which stores the start address of an input data frame in a memory storing the input data frame, and stores a CRC verification result in the start address location; and

an output control unit which with a predetermined offset from the write address, reads the input data frames and if the CRC verification result is normal, output the read data frame.

8. The apparatus of claim 7, wherein the predetermined constant time is the same value as the maximum length of the data frame or a value exceeding the maximum length by a predetermined degree.

9. A CRC verification method having constant delay, comprising:

storing an input data frame and recording the start address in which the data frame is stored;

performing CRC verification of the data frame;

receiving an input control signal, generating a CRC enable signal, generating write address which increases sequentially irrespective of the input of the data frame, and with storing an address in which the start part of the data frame is stored, if input of the data frame finishes, receiving the CRC verification result from the CRC generation unit and storing the CRC verification result in the address in which the start part of the data frame is stored, and providing a read address synchronization signal that makes the read address follow with a predetermined offset after the write address; and

receiving the read address synchronization signal, generating information on a read address which increases sequentially, reading the stored data frame according to this read address information, and according to the CRC result, outputting a different output control signal together with the output data.

10. The method of claim 9, wherein the predetermined length is the same value as the maximum length of the data frame or a value exceeding the maximum length by a predetermined degree.